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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,217	08/26/2003	Yoshitaka Kayukawa	SON-2810	1901

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EXAMINER

GANDHI, DIPAKKUMAR B

ART UNIT PAPER NUMBER

2138

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/647,217	Applicant(s) KAYUKAWA ET AL.	
	Examiner Dipakkumar Gandhi	Art Unit 2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/20/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 3, 5, 8, 10, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashizume (US 6,539,511 B1).

Hashizume anticipates claim 1.

Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; and reset means for resetting said plurality of flip-flops when transitioning from said normal operation mode to said test mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

- Hashizume anticipates claim 2.

Hashizume teaches the semiconductor integrated circuit, wherein said reset means resets said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with said mode signal (fig. 1B, 2, 27, col. 6, lines 45-67, col. 7, lines 31-34, lines 38-42, Hashizume).

- Hashizume anticipates claim 3.

Hashizume teaches the semiconductor integrated circuit, further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test

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mode while prohibiting the outputting of data that is supplied during said normal operation mode (col. 15, lines

- Hashizume anticipates claim 5.

Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; reset means for resetting said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

- Hashizume anticipates claim 8.

Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry (fig. 1A, 1B, 2, col. 5, line 42-col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, Hashizume); and output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode, while prohibiting the outputting of data that is supplied during said normal operation mode (fig. 14, col. 14, lines 55-67, col. 15, lines 11-20, Hashizume).

- Hashizume anticipates claim 10.

Hashizume teaches a method of testing a semiconductor integrated circuit, which has internal logical circuitry and a plurality of flip-flops for scan testing said internal logical circuitry, and which has a normal operation mode and a test mode for performing said scan testing, wherein said plurality of flip-flops are reset when transitioning from said normal operation mode to said test mode (fig. 1A, 1B, 2, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

- Hashizume anticipates claim 11.

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Hashizume teaches a method of testing a semiconductor integrated circuit, which has internal logical circuitry and a plurality of flip-flops for scan testing said internal logical circuitry, and which has a normal operation mode and a test mode for performing said scan testing, wherein said plurality of flip-flops are reset when transitioning from said test mode to said normal operation mode (fig. 1A, 1B, 2, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 4, 9, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 3 above, and further in view of Cavaliere et al. (US 3,961,254).

As per claim 4, Hashizume substantially teaches the claimed invention described in claim 3 (as rejected above).

However Hashizume does not explicitly teach the specific use of the semiconductor integrated circuit, further comprising: memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode in accordance with said mode signal.

Cavaliere et al. in an analogous art teach an LSI semiconductor device comprising a memory array, including address, data and buffer registers (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach

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inhibiting access between the logic circuitry and the memory array when the device is in a test mode (col. 6, lines 26-28, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using the semiconductor integrated circuit, further comprising: memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode in accordance with said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to prevent access to data stored in the memory during the test mode so that the data is not corrupted.

- As per claim 9, Hashizume and Cavaliere et al. teach the additional limitations.

Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, col. 5, line 42-col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, Hashizume).

Cavaliere et al. teach memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal (col. 6, lines 6-8, lines 26-28, Cavaliere et al.).

- As per claim 12, Hashizume and Cavaliere et al. teach the additional limitations.

Hashizume teaches a method of testing a semiconductor integrated circuit, which has internal logical circuitry, a plurality of flip-flops for scan testing said internal logical circuitry and which has a normal operation mode and a test mode for performing said scan testing (fig. 1A, 1B, 2, col. 5, line 42-col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, Hashizume).

Cavaliere et al. teach memory means connected to said plurality of flip-flops, wherein access to said memory means is prohibited during said test mode (col. 6, lines 6-8, lines 26-28, Cavaliere et al.).

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6. Claims 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 1 above, and further in view of Tamamura et al. (US 6,118,316).

As per claim 6, Hashizume substantially teaches the claimed invention described in claim 1 (as rejected above). Hashizume also teaches that the reset means resets said plurality of flip-flops (col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

However Hashizume does not explicitly teach the specific use of the transition detection means for detecting the transition timing of said logical level of said mode signal.

Tamamura et al. in an analogous art teach that as shown in FIG. 3, the pulse generating circuit 5 detects a transition timing (an edge) of the input data 1b, and generates a detected pulse signal 5a so as to be triggered by the transition timing (fig. 3, col. 1, lines 53-56, Tamamura et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Tamamura et al. by including an additional step of using the transition detection means for detecting the transition timing of said logical level of said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the transition detection means for detecting the transition timing of said logical level of said mode signal would provide the opportunity to reset the circuit elements for the new mode of circuit operation.

- As per claim 7, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that the reset means resets said plurality of flip-flops (col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

Tamamura et al. teach transition detection means for detecting the transition timing of said logical level of said mode signal (fig. 3, col. 1, lines 53-56, Tamamura et al.).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Dipakkumar Gandhi
Patent Examiner



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